REMARKS/ARGUMENTS

This amendment responds to the Office Action dated September 28, 2007, in which the Examiner rejected claims 1-28 under 35 U.S.C. § 103.

As indicated above, claims 1, 6, 11 and 18 have been amended for proper antecedent basis and claims 25-28 have been amended for stylistic reasons. The amendments are unrelated to a statutory requirement for patentability and do not narrow the literal scope of the claims.

Claim 1 claims a compression encoder, claim 6 claims a compression-encoding method, claim 11 claims a recorder and claim 18 claims a recording method. The compression encoder, compression method, recorder and recording method comprise dividing input first and second digital input signals, having frame rates different from each other, into plural macro blocks of orthogonal-transformation blocks. The macro blocks are then rearranged by a shuffling section and then compression encoded. The macro blocks of the first digital image are rearranged based on a method of rearranging the macro blocks of the second digital image signals.

By (a) having the first and second digital input signals have different frame rates, and (b) rearranging the macro block of the input first digital image signals based on a method of rearranging the macro blocks of the input second digital image signals, as claimed in claims 1, 6, 11 and 18, the claimed invention provides a compression encoder, compression encoder method, recorder and recording method in which the number of decoders necessary for half-speed reproduction of the first signal can be reduced and deterioration of resolution can be restricted without needing an interpolation processing. The prior art does not show, teach or suggest the invention as claimed in claims 1, 6, 11 and 18.

Claim 25 claims a compression encoder, claim 26 claims a compression-encoding method, claim 27 claims a recorder and claim 28 claims a recording method. The compression encoder, compression-encoding method, recorder and recording method include dividing first and second digital image signals into plural macro blocks. The plural macro blocks of the second digital image signals are rearranged based on a layout of the plural macro blocks of the first digital image signals. The second digital image signals are thus rearranged into a layout of macro blocks which is equivalent to that of the first digital image signals. The rearranged plural macro blocks are then compression-encoded.

By (a) having first and second digital image signals with different frame rates, and (b) rearranging the plural macro blocks of the second digital image signals based on the layout of the plural macro blocks of the first digital image signals so that the second digital image signals are rearranged into a layout of macro blocks that is equivalent to that of the first digital image signals, as claimed in claims 25-28, the claimed invention provides a compression-encoder, compression-encoding method, recorder and recording method which requires no interpolation processing when performing a half-speed reproduction so that resolution can be prevented from deteriorating. Furthermore, only one decoder is necessary during reproduction. The prior art does not show, teach or suggest the invention as claimed in claims 25-28.

Claims 1-2, 4, 6-7, 9, 11-14, 16, 18-21, 23 and 25-28 were rejected under 35 U.S.C. § 103 as being unpatentable over *Miller, et al.* (U.S. Patent No. 5,146,324).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which are set

forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allow the claims to issue

Miller, et al. appears to disclose a block shuffler 10 which accepts luminous data and chrominance data, partitions it into predetermined blocks of data and rearranges the data blocks within each field of video. Such shuffling of data can be performed on either a 1- or 2-dimensional basis. Basically, it aids in distributing the information content of a typical video image more evenly which enhances the performance of the data compression process (Col. 5, lines 11-19).

Thus, *Miller, et al.* only discloses rearranging data blocks within each field of video. Nothing in *Miller, et al.* shows, teaches or suggests how the data blocks are arranged. In particular, nothing in *Miller, et al.* shows, teaches or suggests (a) rearranging macro blocks of an input first digital image signals based on a method of rearranging the macro blocks of the second digital image signal as claimed in claims 1, 6, 11 and 18 and (b) rearranging plural macro blocks of a second digital image signal based on a layout of the plural macro blocks of the first digital image signal so that the second digital image signals are rearranged into a layout of macro blocks which is equivalent to that of the first digital image signals as claimed in claims 25-28. Rather, *Miller, et al.* only discloses rearranging the data blocks but does not show, teach or suggest how they are rearranged or what method is used to rearrange the data blocks.

Additionally, *Miller, et al.* merely discloses a data compression technique for reducing the data rate D_{in} of a digital input signal to a lesser data rate D_{out} of an output data channel (Col. 3, lines 51-54). The input digital video signal 1 represents image data to be compressed,

transmitted over a data channel (or recorded and played back on a recording device), and uncompressed and output as a digital signal 2 (Col. 5, lines 1-5).

Thus, *Miller, et al.* merely discloses an input signal 1 and an output signal 2. Nothing in *Miller, et al.* shows, teaches or suggests inputting first and second digital image signals having frame rates different from each other as claimed in claims 1, 6, 11, 18 and 25-28. Rather, *Miller, et al.* only discloses inputting a digital video signal 1 having the data rate D_{in}, and outputting a digital signal 2 having a lesser data rate D_{out}.

Since nothing in *Miller, et al.* shows, teaches or suggests (a) rearranging macro blocks of a first digital image signal, having a frame rate, based upon a method of rearranging the macro blocks of a second digital image signal having a different frame rate as claimed in claims 1, 6, 11, and 18 and (b) rearranging the plural macro blocks of a second digital image signal, having a frame rate, based on a layout of plural macro blocks of a first digital image signal, having a different frame rate, so that the second digital image signals are rearranged into a layout of macro blocks which is equivalent to that of the first digital image signals, as claimed in claims 25-28, Applicants respectfully request the Examiner withdraws the rejection to claims 1, 6, 11, 18 and 25-28 under 35 U.S.C. § 103.

Claims 2, 4, 7, 9, 12-14, 16, 19-21 and 23 depend from claims 1, 6, 11 and 18 and recite additional features. Applicants respectfully submit that claims 2, 4, 7, 9, 12-14, 16, 19-21 and 23 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Miller, et al.* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 2, 4, 7, 9, 12-14 16, 19-21 and 23 under 35 U.S.C. § 103.

Claims 3, 8, 15 and 22 were rejected under 35 U.S.C. § 103 as being unpatentable over *Miller, et al.*, in view of *Chen, et al.* (U.S. Publication No. 2003/0138051). Claims 5, 10, 17 and 24 were rejected under 35 U.S.C. § 103 as being unpatentable over *Miller, et al.*, in view of *Porter, et al.* (U.S. Patent No. 7,227,900).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in *Miller, et al.* shows, teaches or suggests the primary features as claimed in claims 1, 6, 11 and 18, Applicants respectfully submit that the combination of the primary reference with the secondary reference to *Chen, et al.* or *Porter, et al.* will not overcome the deficiencies of the primary reference. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 3, 5, 8, 10, 15, 17, 22 and 24 under 35 U.S.C. § 103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus, it now appears that the application is in condition for a reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

CONCLUSION

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 05-0320.

Respectfully submitted,

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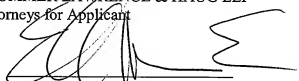
Date: December 17, 2007

By: 
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